

**LOW POWER APPROXIMATE MULTIPLIERS FOR IMAGE PROCESSING APLLICATION**

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**ABSTRACT**

This project focuses on the development and implementation of low-power approximate multipliers tailored for image processing applications. The objective is to design a multiplier architecture that achieves a balance between computational accuracy and power efficiency, crucial for energy-constrained environments and real-time processing. By leveraging techniques such as half adders, full adders, and comparators, the proposed multipliers aim to minimize power consumption while maintaining acceptable levels of accuracy for image processing tasks. Additionally, the project integrates image processing concepts with the developed multiplier architecture, demonstrating its practical utility in tasks such as convolution, filtering, and feature extraction. Through simulation and experimental validation, the proposed approach is evaluated, contributing to the advancement of energy-efficient hardware solutions in the field of image processing.

**Keywords:** Multipliers,Image Processing.